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WF Consulting

UniqueSec ASGARD1

Radar test and verification solution based on FlexRIO and LabVIEW FPGA

AB0005-102, rev A

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"WireFlow delivers efficient LabVIEW FPGA development on time."

– Kasra Haghighi, Founder and CEO, UniqueSec AB

The Challenge

UniqueSec is an innovative company that develops advanced signal processing algorithms for small-scale commercial radars. They design test and verification solutions for radars in different applications, particularly in automotive.

ASGARD1 is a unique radar test and verification solution. The system sits in front of the vehicle or radar under test and emulates electromagnetic emissions analogous to real-scenario radar reflections. The scenario signature updates in response to the vehicle in order to simulate the experience of driving more realistically.

The ASGARD1 radar test and verification solution requires signal generation at 200 MS/s. The signals are connected to 77 GHz RF front-ends.

In the process of creating a prototype implementation of ASGARD1, UniqueSec needed a partner to assist during product development and decrease time to market.

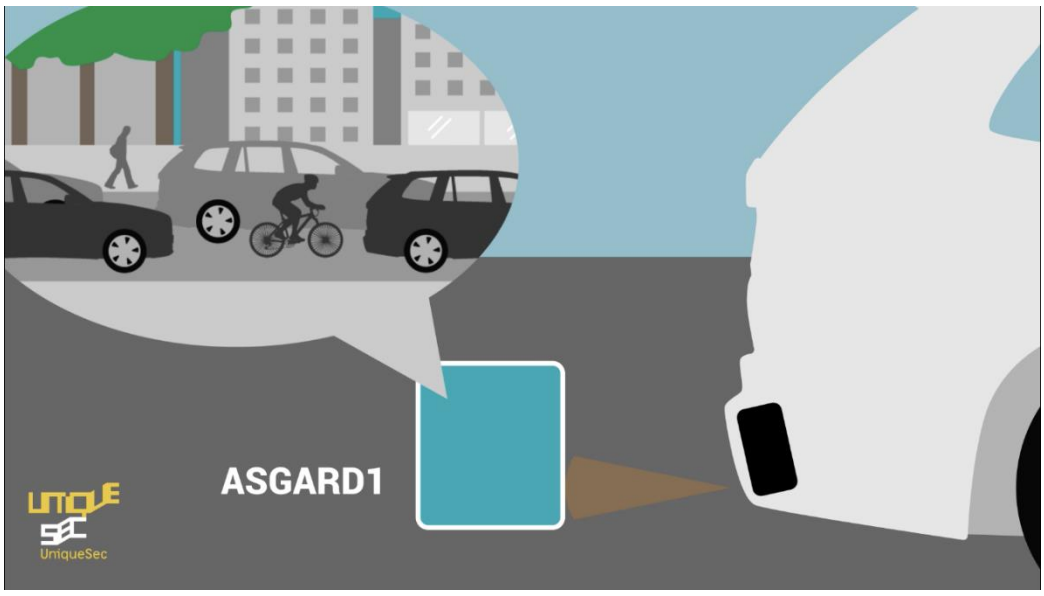

Figure 1. Car radar detects objects simulated by the ASGARD1 system

The Solution

To take on the challenge of designing a powerful and scalable prototype for the ASGARD1 radar test solution, UniqueSec teamed up with National Instruments Alliance partner WireFlow.

For the prototype they decided to use National Instruments FlexRIO together with LabVIEW Real-Time and LabVIEW FPGA. This platform would give the project a powerful tool to quickly design a prototype that could prove the concept of the ASGARD1.

The user of an ASGARD1 system creates test scenarios in a virtual traffic simulator. Scenarios can be set in details by specifying:

- Number and types of vehicles, pedestrians and other road users
- Road and traffic situations
- Environment elements such as guard rails and trees
- Weather conditions

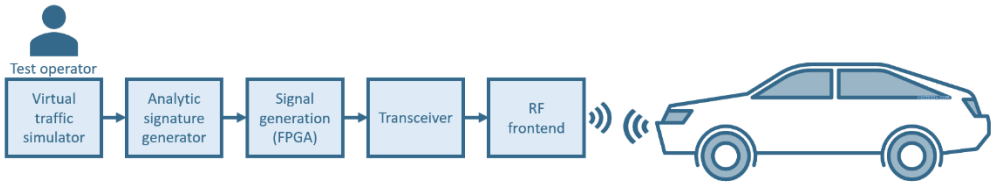

Figure 2. Block diagram of the radar test and verification solution

The ASGARD1 performs an analytic signature generation for the elements defined in the traffic simulator. After this the FPGA is responsible for the signal generation. The signals created by the FPGA are fed into a transceiver which creates the analog signal sent to an RF front-end which transmits the simulated radar echo back to the car.

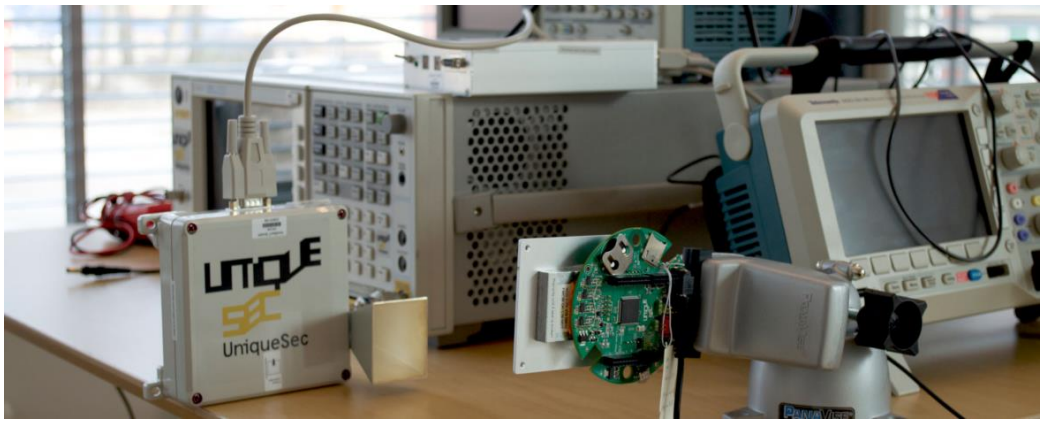

Figure 3. Lab setup of a radar and the ASGARD1 RF frontend

For the prototype WireFlow used the National Instruments FlexRIO, specifically the NI-7935R Controller for FlexRIO paired with the NI-5783 Transceiver Adapter Module. The FlexRIO executes a LabVIEW Real-Time application that sends parameters to the LabVIEW FPGA code that generates 16-bit analog out signals at 200 MS/s.

Figure 4. The FlexRIO FPGA and the Transceiver Adapter Module

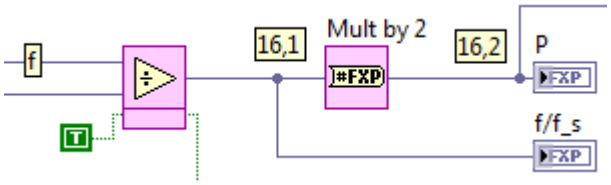

Figure 5. High throughput math in LabVIEW FPGA

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